

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

- 1           1.       (Currently Amended) A circuit for providing write pre-compensation  
2     utilizing read signal timing, comprising:  
3           a first phase clock source for generating a first clock signal having a first phase  
4     and being synchronized with a read signal of the read path;  
5           a second phase clock source for generating a second clock signal having a second  
6     phase at a predetermined phase difference with the first clock signal; and  
7           a write pre-compensation circuit for using the first and second clock signals to  
8     shift write data to achieve write data comprising a first desired pre-compensation;  
9     wherein the second phase clock source generates the second clock signal in  
10  response to a read phase select position signal from the read path and a write phase select  
11  position signal.

- 1           2.       (Canceled)

1           3.       (Currently Amended) The circuit of claim [[ 2 ]] 1, wherein the write pre-  
2       compensation circuit further comprises:  
3           write logic for receiving write data;  
4           a first and second latch, coupled to the write logic, the first and second latch  
5       receiving the write data from the write logic and using the first clock signal to supply a  
6       first data signal and using the second clock signal to supply a second data signal; and  
7           a data selector, coupled to the write logic, for receiving a data select signal from the  
8       write logic and outputting the first or second data signal based on a state of the data select  
9       signal.

1           4.       (Original) The circuit of claim 1, wherein the write pre-compensation  
2       circuit further comprises:  
3           write logic for receiving write data;  
4           a first and second latch, coupled to the write logic, the first and second latch  
5       receiving the write data from the write logic and using the first clock signal to supply a  
6       first data signal and using the second clock signal to supply a second data signal; and  
7           a data selector, coupled to the write logic, for receiving a data select signal from  
8       the write logic and outputting the first or second data signal based on a state of the data  
9       select signal.

1           5.       (Original) The circuit of claim 1 further comprising a coarse phase clock  
2       source, wherein the first and second phase clock sources are first and second fine phase  
3       clock sources, the first and second fine phase clock sources generating the first and  
4       second clock signals based on a coarse phase signal from the coarse phase clock source.

1           6.       (Original) The circuit of claim 1, wherein the second phase clock source  
2       follows the phase of the first clock phase source during a read operation.

1           7.       (Original) The circuit of claim 6, wherein the phase difference between  
2       the second phase clock source and the first phase clock source is maintained.

1           8.       (Original) The circuit of claim 1, wherein the phase difference between  
2       the second phase clock source and the first phase clock source is maintained.

1           9.       (Original) The circuit of claim 1, wherein the first and second phase are  
2       changed to provide write data comprising a second desired pre-compensation.

1           10.      (Original) The circuit of claim 1 further comprising at least one additional  
2       phase clock source, the at least one additional phase clock source providing at least one  
3       additional pre-compensation state.

1           11.     (Currently Amended) A magnetic storage device, comprising:  
2           a magnetic storage medium for recording data thereon;  
3           a motor for moving the magnetic storage medium;  
4           a head for reading and writing data on the magnetic storage medium;  
5           an actuator for positioning the head relative to the magnetic storage medium; and  
6           a data channel for processing encoded signals on the magnetic storage medium,  
7     the data channel comprising a first phase clock source for generating a first clock signal  
8     having a first phase and being synchronized with a read signal of the read path, a second  
9     phase clock source for generating a second clock signal having a second phase at a  
10    predetermined phase difference with the first clock signal and a write pre-compensation  
11    circuit for using the first and second clock signals to shift write data to achieve write data  
12    comprising a first desired pre-compensation, wherein the second phase clock source  
13    generates the second clock signal in response to a read phase select position signal from  
14    the read path and a write phase select position signal.

1           12.     (Canceled)

1           13.     (Original) The magnetic storage device of claim [[ 12 ]] 11, wherein the  
2     write pre-compensation circuit further comprises:  
3           write logic for receiving write data;  
4           a first and second latch, coupled to the write logic, the first and second latch  
5     receiving the write data from the write logic and using the first clock signal to supply a  
6     first data signal and using the second clock signal to supply a second data signal; and  
7           a data selector, coupled to the write logic, for receiving a data select signal from  
8     the write logic and outputting the first or second data signal based on a state of the data  
9     select signal.

1           14.     (Original) The magnetic storage device of claim 11, wherein the write  
2     pre-compensation circuit further comprises:  
3           write logic for receiving write data;  
4           a first and second latch, coupled to the write logic, the first and second latch  
5     receiving the write data from the write logic and using the first clock signal to supply a  
6     first data signal and using the second clock signal to supply a second data signal; and  
7           a data selector, coupled to the write logic, for receiving a data select signal from  
8     the write logic and outputting the first or second data signal based on a state of the data  
9     select signal.

1           15.    (Original) The magnetic storage device of claim 11 further comprising a  
2   coarse phase clock source, wherein the first and second phase clock sources are first and  
3   second fine phase clock sources, the first and second fine phase clock sources generating  
4   the first and second clock signals based on a coarse phase signal from the coarse phase  
5   clock source.

1           16.    (Original) The magnetic storage device of claim 11, wherein the second  
2   phase clock source follows the phase of the first clock phase source during a read  
3   operation.

1           17.    (Original) The magnetic storage device of claim 16, wherein the phase  
2   difference between the second phase clock source and the first phase clock source is  
3   maintained.

1           18.    (Original) The magnetic storage device of claim 11, wherein the phase  
2   difference between the second phase clock source and the first phase clock source is  
3   maintained.

1           19.    (Original) The magnetic storage device of claim 11, wherein the first and  
2   second phase are changed to provide write data comprising a second desired pre-  
3   compensation.

1           20.    (Original) The magnetic storage device of claim 11 further comprising at  
2    least one additional phase clock source, the at least one additional phase clock source  
3    providing at least one additional pre-compensation state.

1           21.    (Currently Amended) A method for providing write pre-compensation  
2    utilizing read signal timing, comprising:  
3           generating a first phase clock signal having a first phase and being synchronized  
4    with a read signal of a read path;  
5           generating a second phase clock signal having a second phase at a predetermined  
6    phase difference with the first clock signal; and  
7           using the first and second clock signals to shift write data to achieve write data  
8    comprising a first desired pre-compensation;  
9           wherein the generating the second clock signal is based on a read phase select  
10   position signal from the read path and a write phase select position signal.

1           22.    (Canceled)

1           23.     (Original) The method of claim [[ 22 ]] 21, wherein the using the first and  
2     second clock signals to shift write data to achieve write data comprising a first desired  
3     pre-compensation further comprises:  
4             receiving write data;  
5             providing the write data to a first latch and a second latch;  
6             using the first clock signal to latch the first latch to supply a first data signal;  
7             using the second clock signal to latch the second latch to supply a second data  
8     signal; and  
9             outputting the first or second data signal based on a state of a received data select  
10    signal.

1           24.     (Original) The method of claim 21, wherein the write pre-compensation  
2     circuit further comprises:  
3             receiving write data;  
4             providing the write data to a first latch and a second latch;  
5             using the first clock signal to latch the first latch to supply a first data signal;  
6             using the second clock signal to latch the second latch to supply a second data  
7     signal; and  
8             outputting the first or second data signal based on a state of a received data select  
9     signal.

1           25.    (Original) The method of claim 21, wherein the generating a first phase  
2 clock signal and generating a second phase clock signal further comprises:  
3           generating a coarse phase clock signal;  
4           generating the first and second phase clock signals based on the coarse phase  
5 clock signal.

1           26.    (Original) The method of claim 21, wherein the generating a first phase  
2 clock signal and generating a second phase clock signal further comprises generating the  
3 second the second phase clock signal with a phase that follows the phase of the first clock  
4 phase signal during a read operation.

1           27.    (Original) The method of claim 26, wherein the generating a first phase  
2 clock signal and generating a second phase clock signal further comprises maintaining  
3 the phase difference between the second phase clock signal and the first phase clock  
4 signal.

1           28.    (Original) The method of claim 21, wherein the generating a first phase  
2 clock signal and generating a second phase clock signal further comprises maintaining  
3 the phase difference between the second phase clock signal and the first phase clock  
4 signal.

1           29.    (Original) The method of claim 21, wherein the generating a first phase  
2   clock signal and generating a second phase clock signal further comprises changing the  
3   phase of the first and second phase clock signals to provide write data comprising a  
4   second desired pre-compensation.

1           30.    (Original) The method of claim 21 further comprising generating at least  
2   one additional phase clock signal for providing at least one additional pre-compensation  
3   state.